



AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

- 1 1. (Previously presented) A computer system comprising a first compo-
2 nent operated in response to timing of a first clock, means for storing informa-
3 tion, means for transferring information from the first component to the means
4 for storing information always utilizing the first clock without synchronization to
5 another clock, a second component operated in response to timing of a second
6 clock, the timing of the first clock being independent of the timing of the second
7 clock, means for utilizing the second clock to transfer information without syn-
8 chronization with the first clock from the means for storing information without
9 transferring other [data] information into said means for storing information
10 whereby the information may be immediately utilized by the second component
11 without need for storage by the second component, said means for utilizing the
12 second clock to transfer information without synchronization with the first clock
13 from said means for storing information comprising means for transferring the
14 information in said means for storing information to the second component un-
15 der control of the second clock, said means for transferring the information in
16 said means for storing information to the second component under control of the

17 second clock includes means for switching the second clock to the terminals used
18 by the first clock, said means for switching the second clock to the terminals used
19 by the first clock includes a multiplexor, said multiplexor coupled to said first
20 component and said second component, said multiplexor receiving a signal from
21 the second component for furnishing a second clock signal from said second
22 clock to said [buffer] means for storing information to transfer [data] information
23 to said second component.

1 2. (Previously presented) A computer system as claimed in claim 1 in
2 which the means for utilizing the clock of the second component to transfer in-
3 formation from [the storage of the first component] the means for storing infor-
4 mation in a condition in which it is synchronized for use by the second compo-
5 nent comprises means for providing a signal to the second component to indicate
6 that a prescribed amount of information has been stored in the [buffer] means for
7 storing information.

1 3. (Previously presented) A computer system as claimed in claim 1, in
2 which the means for switching the second clock to the terminals used by the first
3 clock includes means for signaling the multiplexor that the second component is
4 ready to accept the information in [the buffer] the means for storing information.

1 4. (Previously presented) A computer system comprising a plurality of
2 components operated in response to timing of different clocks, means for storing
3 information, means for utilizing the clock of any one of the components to trans-
4 fer information without synchronization of timing of different clocks between
5 one of the components and the means for storing information, means for signal-
6 ing any of the components that information stored in the means for storing is to
7 be transferred to that one of the components as a destination component, means
8 for utilizing the clock of the destination component to transfer information from
9 the means for storing information without synchronization of timing of different
10 clocks in a condition in which the information is synchronized for use by the des-
11 tination component wherein the means for utilizing the clock of any one of the
12 components always utilizes the clock of the component transferring information
13 into said means for storing information, and wherein the timing of the clock of
14 the component from which the information was transferred is independent of the
15 timing of the clock of the destination component, said means for utilizing the
16 clock of the destination component to transfer information from the means for
17 storing information in a condition in which it is synchronized for use by the des-
18 tination component includes a multiplexor for transferring signals from [ad-
19 dressed components] the destination component to [the means for storage] the

20 means for storing information, said multiplexor coupled to [a first component]
21 the component transferring information into the means for storing information
22 and [a second component] the destination component, said multiplexor receiving
23 a signal from said [second component] the destination component for furnishing
24 a [second] clock signal from [said second clock] the clock of the destination com-
25 ponent to [said buffer] the means for storing information to transfer [data] in-
26 formation to [said second component] the destination component.

1 5. (Previously presented) A computer system as claimed in claim 4 in
2 which the means for [signaling] signaling [another of the components] a second
3 destination component that the information stored in the means for storing in-
4 formation is to be transferred to the [other of the components] second destina-
5 tion component comprises means for synchronizing a signal from the means for
6 signalling [any one of the components] with the clock of the second destination
7 component.

1 6. (Original) A computer system as claimed in claim 4 in which the mul-
2 tiplexor comprises an AND gate, and means for transferring gated clock signals
3 from each of the components as inputs to the AND gate.

1 7. (Previously presented) A computer system as claimed in claim 6 in
2 which the means for transferring gated clock signals from each of the compo-

nents as inputs to the AND gate comprises a plurality of OR gates, each such OR gate connected to receive a clock and a gating signal for transferring the clock from one of the components.

8. (Original) A computer system comprising:

a first component;

a first clock coupled to said first component, said first component operated in response to timing of said first clock;

a buffer coupled to said first component, said first component always using said first clock to transfer data from said first component to said buffer without synchronizing said transfer of said data to another clock;

a second component coupled to said buffer;

a second clock coupled to said second component, the timing of said first clock being independent of the timing of said second clock, said second component reading said data from said buffer using said second clock without synchronizing said reading to another clock and without transferring other data into said buffer;

a multiplexor coupled to said first component and said second component, said multiplexor receiving a signal from the second com-

ponent for furnishing a second clock signal from said second
clock to said buffer to transfer data to said second component.

9. (Original) A computer system as in claim 8 further comprising:

a third component;

a third clock coupled to said third component, said third component
operated in response to timing of said third clock, the timing of
said third clock being independent of the timing of said first
clock,

wherein said first component uses said first clock to transfer further
data from said first component to said buffer without synchro-
nizing said transfer of said further data to another clock, and
wherein said third component transfers said further data from said
buffer using said third clock without synchronizing said trans-
fer of said further data to another clock.

10. (Original) A computer system as in claim 8 further comprising:

a third component;

a third clock coupled to said third component, said third component
operated in response to timing of said third clock the timing of

5 said third clock being independent of the timing of said second
6 clock,

7 wherein said second component uses said second clock to transfer fur-
8 ther data from said second component to said buffer without
9 synchronizing said transfer of said further data to another clock,
10 and

11 wherein said third component transfers said further data from said
12 buffer using said third clock without synchronizing said trans-
13 fer of said further data to another clock.

1 11. (Original) A computer system as in claim 8 wherein said data may be
2 immediately utilized by said second component without storing said data in said
3 second component.

1 12. (Original) A computer system as in claim 9 wherein said further data
2 may be immediately utilized by said third component without storing said fur-
3 ther data in said third component.

1 13. (Original) A computer system as in claim 8 wherein the transfer of
2 said data into said buffer is controlled entirely by said first component and said
3 first clock.

1 14. (Original) A method for transferring data between a plurality of com-
2 ponents in a computer system including a first and a second component, said
3 method comprising:

4 operating said first component using a first clock having a first timing;

5 operating said second component using a second clock having a sec-

6 ond timing independent of said first timing;

7 transferring an entire packet of data having a plurality of words from

8 said first component to a buffer always using said first clock

9 without synchronizing any of said plurality of words to another

10 clock;

11 once said entire packet of data is transferred from said first component

12 to said buffer, signaling said second component that said entire

13 packet of data is ready to be transferred to said second compo-

14 nent;

15 transferring said entire packet of data to said second component using

16 said second clock without transferring other data into said

17 buffer;

18 furnishing a clock signal to said buffer from a multiplexor, said multi-

19 plexor coupled to said first component and said second compo-

20 nent, said multiplexor receiving a signal from the second com-
21 ponent for furnishing a second clock signal from said second
22 clock to said buffer to transfer data to said second component.

1 15. (Original) A method for transferring data as in claim 14, wherein said
2 computer system comprises a third component and wherein said method further
3 comprises:

4 operating said third component using a third clock having a third tim-
5 ing independent of said first clock;

6 transferring a further entire packet of data having a second plurality of
7 words from said first component to said buffer using said first
8 clock without synchronizing any of said second plurality of
9 words to another clock;

10 once said further packet of data is transferred from said first compo-
11 nent to said buffer, signaling said third component that said fur-
12 ther entire packet of data is ready to be transferred to said third
13 component;

14 transferring said further entire packet of data to said third component
15 using said third clock without synchronizing any of said second
16 plurality of words to another clock.

1 16. (Original) A method as in claim 14 wherein said second component
2 uses said entire packet of data immediately without first storing said entire
3 packet of data in said second component.

1 17. (Original) A method as in claim 15 wherein said third component
2 uses said further entire packet of data immediately without first storing said fur-
3 ther entire packet of data in said third component.

1 18. (Original) A method as in claim 15 wherein said step of signaling said
2 second component occurs by broadcasting a first signal from said first compo-
3 nent to said second and third components, said first signal being synchronized to
4 said second clock, and wherein said step of signaling said third component oc-
5 curs by broadcasting a second signal from said first component to said second
6 and third components, said second signal being synchronized to said third clock.

1 19. (Original) A computer system as in claim 8 further comprising:

2 a bus for carrying a first signal, said bus being coupled to said first
3 component and said second component, said first signal being
4 provided by said first component and being synchronized to
5 said second clock, said first signal being received by said second
6 component and causing said second component to read said
7 data from said buffer.

1 20. (Original) A computer system as in claim 9 further comprising:
2 a bus for carrying a first signal and a second signal, said bus being
3 coupled to said first, second and third components, wherein
4 said first signal is provided by said first component and is syn-
5 chronized to said second clock, said first signal being received
6 by said second component and said third component and caus-
7 ing said second component to read said data from said buffer,
8 and wherein said second signal is provided by said first com-
9 ponent and is synchronized to said third clock, said second sig-
10 nal being received by said third component and by said second
11 component and causing said third component to read said fur-
12 ther data from said buffer.

1 21. (Original) A computer system as in claim 19 wherein said data com-
2 prises a plurality of words having a selected number of words and wherein said
3 plurality of words are transferred to said buffer without synchronizing any of
4 said plurality of words to any clock except said first clock and wherein said first
5 signal is received by said second component after all of said plurality of words
6 are transferred to said buffer and wherein all of said plurality of words are trans-

7 ferred to said second component from said buffer after said second component
8 receives said first signal.

1 22. (Original) A computer system as in claim 20 wherein said data com-
2 prises a plurality of words having a selected number of words, and wherein said
3 plurality of words are transferred to said buffer without synchronizing any of
4 said plurality of words to any clock except said first clock and wherein said first
5 signal is received by said second component after all of said plurality of words
6 are transferred to said buffer, and wherein all of said plurality of words are
7 transferred to said second component from said buffer after said second compo-
8 nent receives said first signal, and wherein said further data comprises a further
9 plurality of words, and wherein said further plurality of words are transferred to
10 said buffer without synchronizing any of said further plurality of words to any
11 clock except said first clock and wherein said second signal is received by said
12 third component after all of said further plurality of words are transferred to said
13 buffer and wherein all of said further plurality of words are transferred to said
14 third component from said buffer after said third component receives said sec-
15 ond signal.

1 23. (Currently amended) An apparatus for use in a computer system for
2 transferring data from a first component to a second component, the first com-

3 ponent clocked by a first clock signal, and the second component clocked by a
4 second clock signal, the apparatus comprising:

5 a buffer coupled to the first component and the second component via
6 a data path, the first component always using the first clock sig-
7 nal to transfer data from the first component to the buffer with-
8 out synchronizing the transfer of the data to another clock; and
9 a multiplexer having inputs coupled to the first clock signal and the
10 second clock signal, and an output coupled to the buffer, the
11 multiplexer supplying the first clock signal to the buffer to clock
12 data from the first component to the buffer via the data path in
13 the absence of a valid signal from the second component, and in
14 response to the valid signal from the second component, sup-
15 plying the second clock signal to the buffer to clock data from
16 the buffer to the second component via the data path without
17 transferring other data to the buffer;
18 wherein the timing of the first clock signal is independent of the timing
19 of the second clock signal.

1 24. (Previously presented) The apparatus of claim 23, wherein a ready
2 signal from the first component is transmitted to the second component indicat-
3 ing that the transfer of data from the first component to the buffer is complete.

1 25. (Previously presented) The apparatus of claim 23, wherein the buffer
2 and multiplexer are part of an integrated circuit.

1 26. (Previously presented) A method of transferring data between a first
2 component and a second component in a computer system, the first component
3 clocked by a first clock signal, and the second component clocked by a second
4 clock signal, comprising:

5 clocking data from the first component to a buffer via a data path us-
6 ing the first clock signal in the absence of a valid signal from the
7 first component, the first component always using the first clock
8 signal to transfer data from the first component to the buffer
9 without synchronizing the transfer of the data to another clock;

10 clocking data from the buffer to the second component via the data
11 path using the second clock signal in response to the valid sig-
12 nal from the second component without transferring other data
13 to the buffer; and

14 supplying the first and second clock signals to the buffer via a multi-
15 plexer having a plurality of inputs and an output coupled to the
16 buffer, the inputs for receiving the first and second clock signals
17 and a valid signal from the second component, the multiplexer
18 supplying the second clock signal to the buffer in response to
19 the valid signal;
20 wherein the timing of the first clock signal is independent of the timing
21 of the second clock signal.

1 27. (Previously presented) The method of claim 26, further comprising
2 transmitting a ready signal from the first component to the second component
3 indicating that the transfer of data from the first component to the buffer is com-
4 plete.

1 28. (Previously presented) An apparatus for use in a computer system for
2 transferring data between a plurality of components including at least one source
3 component and at least one destination component, the source component
4 clocked by a first clock signal, and the destination component clocked by a sec-
5 ond clock signal, comprising:

6 a buffer coupled to the source component and the destination compo-
7 nent via a data path, the source component always using the

8 first clock signal to transfer data from the source component to
9 the buffer without synchronizing the transfer of the data to an-
10 other clock;
11 a multiplexer having inputs coupled to the first clock signal and the
12 second clock signal, and an output coupled to the buffer, the
13 multiplexer supplying the first clock signal to the buffer to clock
14 data from the source component to the buffer via the data path
15 in the absence of a gate signal from the destination component,
16 the multiplexer supplying the second clock signal to the buffer
17 to clock data from the buffer to the destination component via
18 the data path in response to the gate signal from the destination
19 component without transferring other data to the buffer; and
20 a broadcast bus coupled to the source component, the destination
21 component and the buffer, the broadcast bus for transferring a
22 ready signal from the source component to the destination
23 component indicating that the transfer of data from the first
24 component to the buffer is complete;
25 wherein the timing of the first clock signal is independent of the timing
26 of the second clock signal.

1 29. (Previously presented) The apparatus of claim 28, wherein the source
2 component places the address of the destination component on the broadcast
3 bus and the destination component supplying the gate signal to the multiplexer
4 in response to the address.

1 30. (Previously presented) The apparatus of claim 28, wherein the buffer
2 and the multiplexer are part of an integrated circuit.